

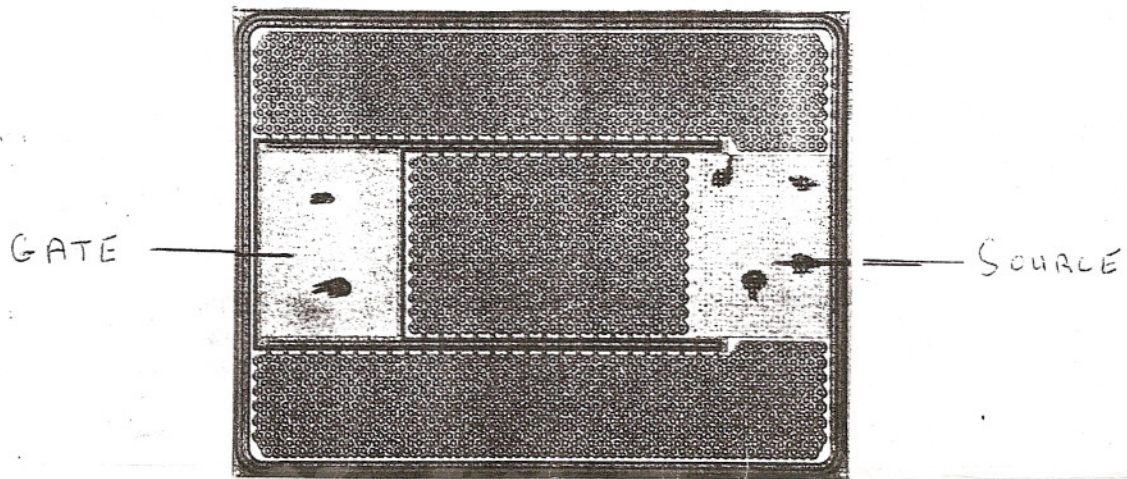


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Topside Metal: Al
Backside: Cr/Ni/Ag
Backside Potential: Drain
Mask Ref: GEN III
Bond Pads : -

APPROVED BY: CD
MFG: Intl. Rectifier

DIE SIZE : .071" x .091"
THICKNESS: -

DATE: 1/6/03
P/N: IRFC9150

DG 10.1.2
Rev A 3-4-99